A Report on Online Webinar "Pre-Silicon RTL Verification using Universal Verification Methodology (UVM) based on 1800.2-2020 IEEE Standard" Program

Date: 25th March 2025

Time: 9 am– 10.30am

Venue: Aryabhatta Seminar Hall, HDL Lab, Dept. of ECE, KSSEM, Bangalore

Target Audiences: Students

No. of Participants: 140 (VI Sem A and B Section, VIII Sem A and B Section)

Online Platform: WebEx

Objective: This webinar is intended to provide insights on the need for UVM & challenges faced by conventional verification approaches using Verilog or System-Verilog. Furthermore, to familiarize students with various base classes, phases and components required to build an UVM Testbench. Illustrating an example Design under Test (DUT), analyzing the steps involved in building & connecting UVM components to generate UVM Test sequences. Finally to create a sample UVM based test plan to achieve verification closure for a given RTL design.

The Department of Electronics and Communication Engineering, KSSEM, in association IEEE student branch and IEEE education Society Bangalore Chapter Region 10, organized an online webinar on "Pre-Silicon RTL Verification using Universal Verification Methodology (UVM) based on 1800.2-2020 IEEE Standard", for the final year and pre final year students of Electronics and Communication Engineering department of KS School of Engineering and Management, on 25th March 2025. The Speaker for the webinar was Dr. Anantharaj Thalaimalai Vanaraj, Formal Verification Leader, Samsung Austin Research Centre – Advanced Computing Lab (SARC-ACL), San Jose, California, USA, and was conducted over WebEx Meetings.

The Registration QR code was open from 18th march 2025. 403 registrations were received from students, faculty, and Industry professionals across Karnataka and two participants outside India. 244 participants attended the webinar.

The webinar began with the welcome speech by Dr. Renuka V Tali, IEEE student branch counselor followed by brief introduction of speaker. The session began with Pre-Silicon RTL Verification, UVM – An Introduction, UVM Test Bench (TB) Basic Building Blocks, UVM-TB Architecture and finally with an example code of Creating an UVM Testbench. The questionnaire session was very interactive as many career related questions were asked by the students. Dr. Anantharaj also shared few links of resources related to UVM that could help students begin their VLSI verification journey.

Fig 1: Webinar poster

Fig 2: Students attending the webinar

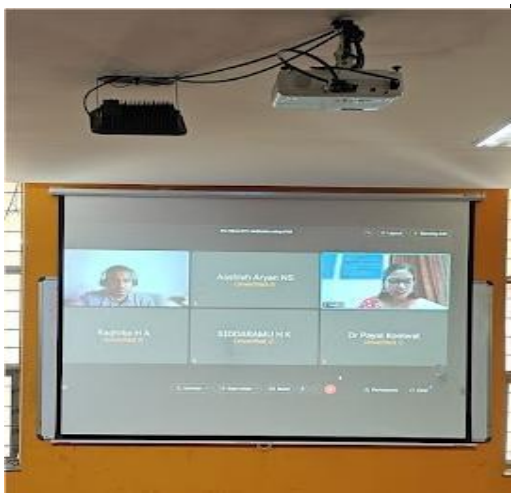

Fig 3: Online through WebEx meeting

Fig 4: Students understanding the UVM Concepts

Outcome:

- The participants gained insights on Pre-silicon RTL verification improvements, tools, and methodologies.
- Participants were introduced to the verification framework, basic building blocks like structural, behavioral and operational blocks.
- Participants were exposed to UVM testbench architecture with sample codes on UVM Sequence item, sequence and sequencer, driver, monitor and scoreboard classes.
- Typical UVM agent, environment and top test bench and their interfacing discussed during webinar created interest and paved the way to begin their RTL verification journey.

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