Sample copy of Question Paper

K.S. SCHOOL OF ENGINEERING AND MANAGEMENT, BANGALORE - 560109
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SESSION: 2021-2022 (ODD SEMESTER)
I SESSIONAL TEST QUESTION PAPER
SET-A

USN

Degree	:	B.E	Semester :	III
Branch	:	Electronics and Communication Engineering	Course Code :	18EC34
Course Title	:	Digital System Design	Date :	03/12/2021
Duration	:	90 Minutes	Max Marks :	30

Note: Answer ONE full question from each part.

Q No.	Question	Marks	K-Level	CO mapping
	PART-A			
1(a)	**Determine** the minimal SOP form of f(A,B,C,D) = Σm (0,1,2,3,6,7,8,9,14,15) using K-Map method.	5	Applying (K3)	CO1
(b)	**Develop** suitable logic circuit to implement the logic function determined in 1 a) using only NAND gates.	5	Applying (K3)	CO1
(c)	**Design** a 4:2 priority encoder with a valid output.	5	Applying (K3)	CO2
	OR			
2(a)	**Determine** the minimal POS form of f(A,B,C,D) = πM (0,1,2,3,6,8,9,14,15) +Σd(7,12)using K-map method.	5	Applying (K3)	CO1
(b)	**Develop** suitable logic circuit to implement the logic function determined in 2 a) using only NOR gates.	5	Applying (K3)	CO1
(c)	**Design** a 4-bit binary to gray converter and realize it using XOR gates.	5	Applying (K3)	CO2
	PART-B			
3(a)	**Determine** the canonical form for following: f1 = A + BC + AC'D f2 = A(B+C')(A+C'+D)	5	Applying (K3)	CO1
(b)	**Develop** suitable logic circuit to implement the logic functions in 3 a) using only NAND and/or NOR gates.	5	Applying (K3)	CO1
(c)	**Establish** the following Boolean function using 3 to 8 decoder with active high enable and active high output, f(A,B,C,D) = Σm (0,3,6,9,12,15).	5	Applying (K3)	CO2
	OR			
4(a)	**Determine** the minimal SOP form of f(A,B,C,D) = Σm (1,3,6,8,9,10,12,14) +Σd(7,13)using Quine-McClusky method.	5	Applying (K3)	CO1
(b)	**Develop** suitable logic circuit to implement the logic function determined in 4 a) using only NAND gates.	5	Applying (K3)	CO1
(c)	**Establish** the following Boolean function using 74138 f(A,B,C,D) = Σm (1,3,7,9,14,15).(74138 has two active low and one active high enable inputs and produces active high output).	5	Applying (K3)	CO2

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I SESSIONAL TEST QUESTION PAPER
SET-B

USN

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Course Title	:	Digital System Design	Date	: 03/12/2021
Duration	:	90 Minutes	Max Marks	: 30

Note: Answer ONE full question from each part.

Q No.	Question	Marks	K-Level	CO mapping
	PART-A			
1(a)	**Determine** the minimal POS form of f(A,B,C,D) = Σ m (2,3,4,10, 13,14,15) +Σd(7,9,11) using K-map method.	5	Applying (K3)	CO1
(b)	**Develop** suitable logic circuit to implement the logic function determined in 2 a) using only NAND gates.	5	Applying (K3)	CO1
(c)	**Design** a 4-bit Excess-3 to BCD converter and realize it using basic gates.	5	Applying (K3)	CO2
	OR			
2(a)	**Determine** the minimal POS form of f(A,B,C,D) = πM (0,1,2,4,5,8,9,10,14,15) +Σd(3,13) using K-map method.	5	Applying (K3)	CO1
(b)	**Develop** suitable logic circuit to implement the logic function determined in 2 a) using only NOR gates.	5	Applying (K3)	CO1
(c)	**Design** a 4 gray to binary converter and realize it using suitable gates.	5	Applying (K3)	CO2
	PART-B			
3(a)	**Determine** the minimal form of f(A,B,C,D) = Σ m (3,4,7,10,12,14,15) +Σd(2,11) using Quine-McClusky method.	5	Applying (K3)	CO1
(b)	**Develop** suitable logic circuit to implement the logic function determined in 2 a) using only NAND gates.	5	Applying (K3)	CO1
(c)	**Establish** the following Boolean function using 74139 dual 2:4 decoder f(A,B,C) = πM (1,3,5,7) (74139 has an active low enable and active low outputs)	5	Applying (K3)	CO2
	OR			
4(a)	**Determine** the minimal form of f(A,B,C,D) = Σ m (0,2,3,8,9,14,15) +Σd(1,5,12)using Quine-McClusky method.	5	Applying (K3)	CO1
(b)	**Develop** suitable logic circuit to implement the logic function determined in 4 a) using only NAND gates.	5	Applying (K3)	CO1
(c)	**Establish** the following Boolean function using 74138 f(A,B,C,D) = Σm (0 ,2,6, 10,12,15).(74138 has two active low and one active high enable inputs and produces active high output)	5	Applying (K3)	CO2

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II SESSIONAL TEST QUESTION PAPER
SET-A

USN | | | | | | | | | | |

Degree	:	B.E	Semester	:	III
Branch	:	Electronics and Communication Engineering	Course Code	:	18EC34
Course Title	:	Digital System Design	Date	:	13/01/2022
Duration	:	90 Minutes	Max Marks	:	30

Note: Answer ONE full question from each part.

Q No.	Question	Marks	K-Level	CO mapping
	PART-A			
1(a)	**Design** a 8-bit magnitude comparator using 7485 ICs.	5	Applying (K3)	CO2
(b)	**Construct** a clocked D flip flop using NAND gates and explain it's operation with necessary truth table and waveforms.	5	Applying (K3)	CO3
(c)	**Design** a 3 bit synchronous counter using JK flip flops and explain it's operation with necessary waveforms and truth table.	5	Applying (K3)	CO3
	OR			
2(a)	Explain the working of carry look ahead adder and **obtain** expression for carry propagate and carry generate functions	5	Applying (K3)	CO2
(b)	**Construct** a MS-JK flip flop using only NAND gates and explain it's operation.	5	Applying (K3)	CO3
(c)	**Develop** a switch debouncer using SR flip flop and explain it's operation with necessary waveforms.	5	Applying (K3)	CO3
	PART-B			
3(a)	**Develop** a function generator to generate the function f(a,b,c,d) = Σm(0,4,8,10,14,15) using 8:1 Mux with a,b,c as select lines.	5	Applying (K3)	CO2
(b)	**Construct** a 4-bit ring counter using JK flip flops and explain it's working using relevant waveforms.	5	Applying (K3)	CO3
(c)	**Explain** the universal shift register with relevant logic diagram and the truth table.	5	Understanding (K2)	CO3
4(a)	Explain the structure of programmable logic arrays (PLA) and **construct** any SOP function using PLA.	5	Applying (K3)	CO2
(b)	**Obtain** characteristic equation for J-K and T flip flops.	5	Applying (K3)	CO3
(c)	**Explain** the PISO and PIPO operation of shift register with relevant logic diagram and the truth table.	5	Understanding (K2)	CO3

(5)

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II SESSIONAL TEST QUESTION PAPER
SET-B

USN

Degree	:	B.E	Semester	: III
Branch	:	Electronics and Communication Engineering	Course Code	: 18EC34
Course Title	:	Digital System Design	Date	: 13/01/2022
Duration	:	90 Minutes	Max Marks	: 30

Note: Answer ONE full question from each part.

Q No.	Question	Marks	K-Level	CO mapping
	PART-A			
1(a)	**Develop** an 8-bit parallel adder/subtractor using 7483 ICs.	5	Applying (K3)	CO2
(b)	**Construct** a MS-JK flip flop using only NAND gates and explain it's operation.	5	Applying (K3)	CO3
(c)	**Design** a 3 bit asynchronous up-down counter using JK flip flops and explain it's operation with necessary waveforms and truth table.	5	Applying (K3)	CO3
	OR			
2(a)	**Establish** a carry look ahead adder and **obtain** expression for carry propagate and carry generate functions.	5	Applying (K3)	CO2
(b)	**Construct** a clocked SR flip flop using NAND gates and explain it's operation with necessary truth table and waveforms.	5	Applying (K3)	CO3
(c)	**Develop** a 4-bit twisted ring counter and explain it's working using relevant waveforms.	5	Applying (K3)	CO3
	PART-B			
3(a)	**Develop** a function generator to generate the function f(a,b,c,d) = Σm(0,4,8,10,14,15) using 4:1 Mux with a,b as select lines.	5	Applying (K3)	CO2
(b)	**Obtain** characteristic equation for J-K and D flip flops.	5	Applying (K3)	CO3
(c)	**Explain** the SISO and SIPO operation of shift register with relevant logic diagram and the truth table.	5	Understanding (K2)	CO3
	OR			
4(a)	**Design** a 2-bit magnitude comparator and implement it using basic gates.	5	Applying (K3)	CO2
(b)	**Construct** a 4-bit ring counter using D flip flops and explain it's working using relevant waveforms.	5	Applying (K3)	CO3
(c)	**Explain** the universal shift register with relevant logic diagram and the truth table.	5	Understanding (K2)	CO3

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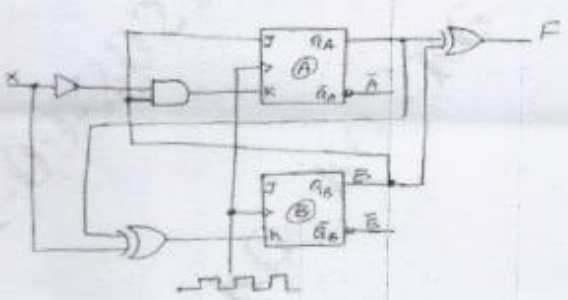
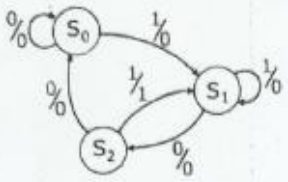
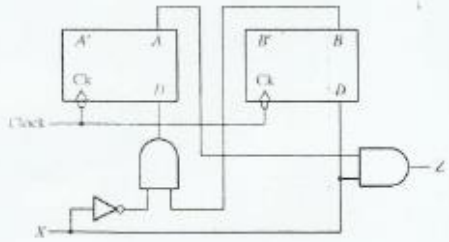
Degree	:	B.E	Semester	:	III
Branch	:	Electronics and Communication Engineering	Course Code	:	18EC34
Course Title	:	Digital System Design	Date	:	15/03/2022
Duration	:	90 Minutes	Max Marks	:	30

Note: Answer ONE full question from each part.

Q No.	Question	Marks	K-Level	CO mapping
	PART-A			
1(a)	**Design** a synchronous decade counter using JK Flip Flops.	10	Applying (K3)	CO4
(b)	**Design** a Moore type Sequence detector to detect a serial input sequence of 1101.	5	Applying (K3)	CO5
	OR			
2(a)	A sequential circuit with 2JK Flip Flop A and B and input X and output F is shown in fig 2(a).  Fig 2(a) i. **Derive** the state table. ii. **Construct** the state diagram. iii. What functionality is achieved by this circuit?	10	Applying (K3)	CO4
(b)	**Develop** the state model for BCD to excess-3 code converter.	5	Applying (K3)	CO5
	PART-B			
3(a)	**Design** a clocked sequential circuit which operates according to the state diagram shown in fig below. Implement the circuit using negative edge triggered J-K Flip Flops.	10	Applying (K3)	CO4

	 Fig 3(a)			
(b)	Develop a serial adder with accumulator to add two 4 bit numbers.	5	Applying (K3)	CO5
4(a)	Develop the state model for circuit shown in fig 4(a):  Fig 4(a)	10	Applying (K3)	CO4
(b)	Design a Mealy type Sequence detector to detect a serial input sequence of 1101.	5	Applying (K3)	CO5

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III SESSIONAL TEST QUESTION PAPER
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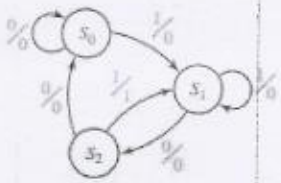
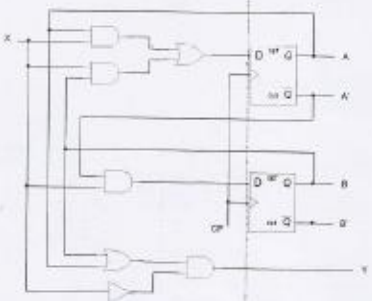
Course Title	:	Digital System Design	Date	: 15/03/2022
Duration	:	90 Minutes	Max Marks	: 30

Note: Answer ONE full question from each part.

Q No.	Question	Marks	K-Level	CO mapping
	PART-A			
1(a)	**Design** a mod 6 self correcting synchronous counter using D Flip Flops to count the sequence 0,2,3,6,5,1,0,...	10	Applying (K3)	CO4
(b)	**Design** a Moore type Sequence detector to detect a serial input sequence of 1101.	5	Applying (K3)	CO5
	OR			
2(a)	**Develop** the state model for clocked sequential circuit which operates according to the state diagram shown in fig 2(a) and **build** it using D flip flops.  Fig 2(a)	10	Applying (K3)	CO4
(b)	**Design** a Mealy type Sequence detector to detect a serial input sequence of 101.	5	Applying (K3)	CO5
	PART-B			
3(a)	 Fig 3(a)	10	Applying (K3)	CO4

	A sequential circuit with 2D Flip Flop A and B and input X and output Y is shown in fig 3(a). **Develop** the state model and state diagram.			
(b)	With the help of neat block diagram **explain** the operation of serial adder with accumulator.	5	**Understanding (K2)**	CO5
4(a)	**Design** a Mealy type Sequence detector to detect a serial input sequence of 101 in a given sequence of 001101100101011.	10	**Applying (K3)**	CO4
(b)	**Differentiate** between Moore and Mealy models with the help of suitable block diagrams.	5	**Understanding (K2)**	CO5

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