

K.S. SCHOOL OF ENGINEERING AND MANAGEMENT, BANGALORE - 560109 DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING SESSION: 2022-2023 (ODD SEMESTER)

III SESSIONAL TEST QUESTION PAPER SET-A

USN

Degree

: B.E

Electronics and Communication Engineering

Semester: III A & B Course Code: 21EC32

Branch Course Title

: Digital System Design Using Verilog

Date: 21EC32

Course Title Duration

: Digital System Des

Max Marks: 20

Note: Answer ONE full question from each part.

Q No.	Question	Marks	K- Level	CO mapping
	PART-A			
1(a)	Illustrate with examples Verilog Arithmetic operators giving operator symbol, description and result type.	5	Understanding (K2)	
(b)	Construct a Verilog code in structural modeling style to realize full subtractor using gates.	5	Applying (K3)	CO5
	OR	9 %		
2(a)	Elaborate with examples Verilog data-types: nets and registers.	5	Understanding (K2)	CO4
(b)	Construct a Verilog code in structural modeling style to realize Boolean expression f(a,b,c)=a'bc+ab'c' using gates.	5	Applying (K3)	CO5
	PART-B			
3(a)	Develop a Verilog code to realize 2X1 mux with active low enable in dataflow modeling style.	5	Applying (K3)	CO4
(b)	Explain the structure of Verilog HDL behavioral description with example.	5	Understanding (K2)	CO5
	OR			1
4(a)	Model a Verilog code to realize full adder in dataflow modeling style.	5	Applying (K3)	CO4
(b)	Explain Verilog IF and ELSE-IF statements with suitable example for each.	5	Understanding (K2)	CO5

ourse Incharge

HOD

IQAC-Coordinator

Principal

Professor & Head

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K.S. SCHOOL OF ENGINEERING AND MANAGEMENT, BANGALORE - 560109 DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SESSION: 2022-2023 (ODD SEMESTER) III SESSIONAL TEST QUESTION PAPER SET-B

USN

Degree

Electronics and Communication Engineering

Semester:

III A & B

Branch

Course Code:

21EC32

Course Title

Digital System Design Using Verilog

Date:

27/03/2023

Duration

60 Minutes

Max Marks:

20

Note: Answer ONE full question from each part.

Q No.	Question	Marks	K- Level	CO mapping	
	PART-A				
1(a)	Explain with examples Verilog logical bitwise operators giving operator symbol, gate, operand type and result type.	5	Understanding (K2)	CO4	
(b)	Construct a Verilog code in structural modeling style to realize Boolean expression f(a,b,c)=a'bc+ab'c' using gates.	5	Applying (K3)	CO5	
	OR				
2(a)	Elaborate with examples Verilog data-types: vectors and arrays.	5	Understanding (K2)	CO4	
(b)	Construct a Verilog code in structural modeling style to Apply		Applying (K3)	CO5	
	PART-B				
3(a)	Model a Verilog code to realize 2X4 decoder in dataflow modeling style.	5	Applying (K3)	CO4	
(b)	Construct a behavioral description Verilog code for a positive edge triggered JK flip-flop using the case statement.	5	Applying (K3)	CO5	
	OR				
4(a)	Develop a Verilog code to realize full subtractor in dataflow modeling style.	5	Applying (K3)	CO4	
(b)	Construct a behavioral description Verilog code for a 3 bit binary counter using the case statement.	5	Applying (K3)	CO5	

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SESSION: 2022-2023 (ODD SEMESTER) III SESSIONAL TEST QUESTION PAPER SET-A

USN

Degree

B.E

Branch

Electronics & Communication Engineering

Semester:

III A & B

Course Title Duration

Basic Signal Processing

60 Minutes

Course Code: 21EC33

Date: 28/03/2023

Max Marks: 20

Note: Answer ONE full question from each part.

Q No.	Question	Marks	K- Level	CO mapping
	PART-A			
1(a)	Explain the different properties of convolution sum with appropriate equations and examples.	5	Understanding (K2)	CO4
(b)	Determine the Z-Transform of $x(n) = \left(\frac{1}{2}\right)^n u(n)$ and Find the ROC.	5	Applying (K3)	CO5
	OR			
2(a)	Explain the following properties of LTI System in terms of Impulse response, with appropriate equations: Causality ii) Stability iii) Memory	5	Understanding (K2)	CO4
(b)	Determine the inverse Z transform using partial fraction method: $X(z) = \frac{z^2}{(z-1)(z-\frac{1}{2})}$	5	Applying (K3)	CO5
	PART-B			
3(a)	Determine the convolution of 2 sequences $x_1(n)$ and $x_2(n)$ by Graphical method: $x_1(n) = \{1,2,3\}$ $x_2(n) = \{2,1,4\}$	5	Applying (K3)	CO4
(b)	Using the properties of Z transform, Determine the Z transform of: a) $x(n) = u(-n+1)$ b) $x(n) = n\alpha^n u(n)$	5	Applying (K3)	CO5
	OR			
4(a)	Determine the discrete time convolution sum of $y(n) = u(n) * u(n - 3)$	5	Applying (K3)	CO4
(b)	Determine the Z transform of the signal and sketch ROC for: $x(n) = \left(\frac{1}{3}\right)^n sin\left(\frac{\pi}{4}n\right)$	5	Applying (K3)	CO5

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K.S. SCHOOL OF ENGINEERING AND MANAGEMENT, BANGALORE - 560109 DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

USN

SESSION: 2022-2023 (ODD SEMESTER) III SESSIONAL TEST QUESTION PAPER SET-B

Degree Branch B.E

Electronics & Communication Engineering

Semester: III A & B

Course Code: 21EC33

Date: 28/03/2023

Course Title Duration

Basic Signal Processing 60 Minutes

Max Marks: 20

Note: Answer ONE full question from each part.

Q No.	Question	Marks	K- Level	CO mapping
	PART-A			
1(a)	Explain the following properties of LTI System in terms of Impulse response, with appropriate equations: i) Causality ii) Stability iii) Memory	5	Understanding (K2)	CO4
(b)	Determine the Z transform of the signal and sketch ROC for $x(n) = \left(\frac{1}{3}\right)^n \sin\left(\frac{\pi}{4}n\right)$	5	Applying (K3)	CO5
	OR			
2(a)	Explain the different properties of convolution sum with appropriate equations and examples.	5	Understanding (K2)	CO4
(b)	Determine the inverse Z transform and Sketch ROC for the given conditions: $X(z) = \frac{z(z^2 - 4z + 5)}{(z - 3)(z - 2)(z - 1)}$ i) $2 < z < 3$ ii) $ z > 3$ iii) $ z < 1$	5	Applying (K3)	CO5
	PART-B			
3(a)	Determine the discrete time convolution sum of $y(n) = u(n) * u(n-3)$	5	Applying (K3)	CO4
(b)	$y(n) = u(n) * u(n-3)$ Determine the Z-Transform of $x(n) = \left(\frac{1}{2}\right)^n u(n)$ and Find the ROC.	5	Applying (K3)	CO5
	OR			
4(a)	Determine the convolution of 2 sequences $x_1(n)$ and $x_2(n)$ by Graphical method $x_1(n) = \{1,2,0.5,1\}$ $x_2(n) = \{1,2,1,-1\}$	5	Applying (K3)	CO4
(b)	Using the properties of Z transform, Determine the Z transform of a) $x(n) = u(-n-2)$ b) $x(n) = 2^n u(n-2)$	5	Applying (K3)	CO5

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K.S. SCHOOL OF ENGINEERING AND MANAGEMENT, BANGALORE - 560109 DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SESSION: 2022-2023 (ODD SEMESTER) III SESSIONAL TEST QUESTION PAPER SET-A

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Degree Branch

B.E

Semester: III

Course Title

Electronics and Communication Engineering Analog Electronics Circuits

Course Code: 21EC34

Date: 28/03/2023

Duration

60 Minutes

Max Marks: 20

Note: Answer ONE full question from each part

Q No.	Note: Answer ONE full question fr Question	Marks	K- Level	CO mapping
	PART-A			
1(a)	Explain 4-Bit binary weighted D/A converter with the help of a circuit. Calculate output voltage for binary values of $b_3b_2b_1b_0$ =0011and $b_3b_2b_1b_0$ =1111. Given R_F =R=10K Ω and V_{ref} =5 V.	5	Applying (K3)	CO4
(b)	Define Power Electronics and explain with functional block diagram.	5	Understanding (K2)	CO5
	Explain the first order by			
2(a)	Explain the first order butter worth low pass filter with neat circuit diagram and frequency response. Derive the expression for $\frac{V0}{Vin}$.	5	Applying (K3)	CO4
(b)	Explain V-I characteristics of SCR.	5	Understanding (K2)	CO5
	PART-B	1	(12)	
3(a)	Design a narrow bandpass filter with two feedback paths with f_c =1.5kHz, Q=7 and A_F =15. Calculate new value of the resistance in the circuit which will change f_c to 2kHz.	5	Applying (K3)	CO4
(b)	Explain different Power Electronics converter circuits and mention two applications for each.	5	Understanding	COF
	OR		(K2)	CO5
(a)	Explain the operation of 555 timer as an Astable multivibrator and design the same for 50% duty cycle.	5	Applying	CO.4
h)	Explain Class A commutation circuit with neat circuit diagram and waveforms.	5	(K3) Understanding	CO4

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SESSION: 2022-2023 (ODD SEMESTER) III SESSIONAL TEST QUESTION PAPER SET-B

USN					

Degree Branch B.E

Electronics and Communication Engineering

Semester:

Course Code: 21EC34

Course Title

Analog Electronics Circuits

Date: 28/03/2023

Duration

60 Minutes

Max Marks:

ONE full question from each part

	Note: Answer ONE full question fr	om eacn	parı.			
Q No.	Question	Marks	K- Level	CO mapping		
	PART-A					
1(a)	Explain 4-Bit R-2R ladder network D/A converter with the help of a circuit. Calculate output voltage for binary values of $b_3b_2b_1b_0$ =1000 and $b_3b_2b_1b_0$ =1111. Given R_F =20K Ω , R =10K Ω and V_{ref} =5 V.	ate output voltage for 00 and $b_3b_2b_1b_0=1111$. $1 V_{ref}=5 V$.				
(b)	Define Power Electronics and explain with functional block diagram.	5	Understanding (K2)	CO5		
	OR					
2(a)	Design first order High pass filter with cut off frequency of 10 KHz with pass band gain of 1.5. Also plot the frequency response for the designed filter.	5	Applying (K3)	CO4		
(b)	Explain any two Thyristors turn on methods.	5	Understanding (K2)	CO5		
	PART-B		,			
3(a)	Design a narrow bandpass filter with two feedback paths with f_c =1.5kHz, Q=7 and A_F =15. Calculate new value of the resistance in the circuit which will change f_c to 2kHz.	5	Applying (K3)	CO4		
(b)	Explain different Power Electronics converter circuits and mention two applications for each.	5	Understanding (K2)	CO5		
	OR					
4(a)	Explain the operation of 555 timer as a Monostable multivibrator and derive the expression for pulse width T.	xplain the operation of 555 timer as a Monostable sultivibrator and derive the expression for pulse width T. Applying (K3)				
(b)	Explain the operation of RC-triggering circuit with _ Understanding					

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